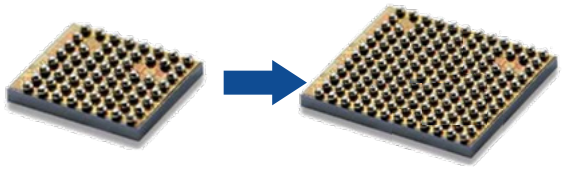


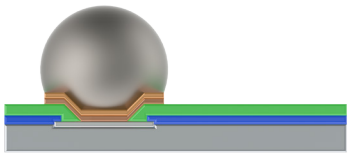
Wafer Level Processing & Die Processing Services (WLP/DPS)

Amkor offers Wafer Level Chip Scale Packaging (WLCSP) providing a solder interconnection directly between a device and the motherboard of the end product. WLCSP includes wafer bumping (with or without pad layer redistribution or RDL), wafer level final test, device singulation and packing in tape & reel to support a full turnkey solution. Amkor's robust Under Bump Metallurgy (UBM) over PBO or PI dielectric layers on the die active surface providing a reliable interconnect solution able to survive harsh board level conditions meeting the demands of the growing global consumer market place for portable electronics.

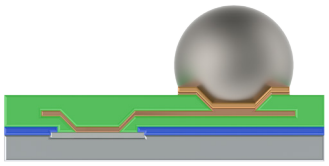
Fueling Growth

- Small packages in mobile are critical to maximize battery size
- Level of adoption in fastest growing markets (i.e., tablets and smartphones)
- Dis-integration of high performance functions from processors to new specialized devices(e.g., audio)
- Fewer cycles through electrical test
- Lower cost to EMS assembly MSL L1 package from T&R
- Improved SMT-compatible underfill processes at EMS companies increase prior die size limits

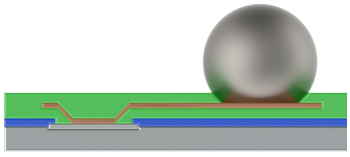
The **CSP^{nl} Bump on Repassivation (BoR)** option provides a reliable, cost-effective, true chip size package on devices not requiring redistribution. The BoR option utilizes a repassivation polymer layer with excellent electrical/mechanical properties. A UBM is added, and solder bumps are then placed directly over die I/O pads. CSPnl is designed to utilize industry-standard surface mount assembly and reflow techniques.



WLCSP



The **CSP^{nl} Bump on Redistribution** option adds a plated copper Redistribution Layer (RDL) to route I/O pads to JEDEC/EIAJ standard pitches, avoiding the need to redesign legacy parts for CSP applications. A nickel-based or thick copper UBM offerings, along with polyimide or PBO dielectrics, provide best in class board level reliability performance. CSPnl with RDL utilizes industry-standard surface mount assembly and reflow techniques, and does not require underfill on qualified device size and I/O layouts.



The **CSP^{n3}** option utilizes one layer of copper for both redistribution and UBM. This simplified process flow reduces cost and cycle time by over 20%. CSPn3 has been in production since 2009 and as of 2015 has a run rate of over 2.8 billion units since its introduction.

Applications

The WLCSP package family is applicable for a wide range of semiconductor device types from high end RF WLAN combo chips, to FPGAs, power management, Flash/EEPROM, integrated passive networks and standard analog. WLCSP offers the lowest total cost of ownership enabling higher semiconductor content while leveraging the smallest form factor and one of the highest performing, most reliable, semiconductor package platforms on the market today. WLCSP is ideally suited for, but not limited to, mobile phones, tablets, netbook PCs, disk drives, digital still & video cameras, navigation devices, game controllers, other portable/remote products and some automotive end applications.

Wafer Level Features

- 4-196 ball count
- Small body 0.64 mm^2 to large 50.0 mm^2 body size
- PBO & Polyimide (PI) Repassivation and Redistribution Layer (RDL) available
- Electroplated Sn/Ag < 0.3 µm and SAC Alloy ball-loaded bumping options ≥ 0.3 µm pitch
- Reliable thick Cu UBM or Ni/Au for best in class EM performance
- Compatible with conventional SMT assembly and test techniques

Die Level Features

- Best in class component and board level reliability
- JEDEC tested board level performance demonstrated without underfill
- Precision edge quality ensuring device integrity at board mount
- Back-side laminate coating available
- Cost effective T&R packaging solutions for small ICs
- Ultra-thin backgrinding for embedded die applications
- Full turnkey WLP, contact probe and DPS supported in Taiwan, China and Korea
- Wide selection of pocket tape carrier options

Visit Amkor Technology online for locations and to view the most current product information.

WLCSP

Package Options

Ball Loading	Pitch	Sphere Diameter
	0.50 mm	0.30 mm
	0.40 mm	0.25 mm
	0.30 mm	0.20 mm

Reliability Qualification

Package Level:

- Preconditioning at Level 1 (Unlimited out of bag life) — 85°C/85% RH, 168 hours, reflow @ 260°C peak
- Temp Cycle — -55°C/+125°C, 1000 cycles
- High Temp Storage — 150°C, 1000 hours

Board Level:

- Temp Cycle — -40°C/+125°C, 15 min. ramp rate, ≥ 500 cycles
- Drop Test — JEDEC condition B (1500G), ≥ 100 drops

Process Highlights

- Die thickness — 150 µm* to 450 µm
- Bump height — 0.5 mm Pitch: 250 µm
0.4 mm Pitch: 210 µm
0.3 mm Pitch: 170 µm
- Solder ball pitch (ball loaded)
Pitch (plated) — 0.28, 0.3, 0.35, 0.4, 0.5 mm
0.12 to 0.25 mm
- Solder sphere diameter — 0.2, 0.25, 0.3 mm
- Redistribution trace/space (min) — CSPnl: 12/12 µm
CSPn3: 15/15 µm
- Via diameter (min) — PBO: 15 µm
Polyimide: 25 µm
- Backside laminate (black) — Available
- Saw street (min) — 65 µm (passivation free space)

Standard Materials

- Dielectric materials — PBO and polyimide, cure polymers, low cure polymers
- RDL metalization — Plated copper
- UBM — Thick Cu or Ni-based
- Solder composition (ball loaded)
(plated) — Pb-free SAC alloys
Sn/Ag Pb-free, Cu pillar

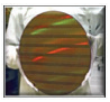
Shipping

Carrier tape — 7″, 13″ reels

*Advanced manufacturing rules may be required. Contact Amkor Business Unit for additional information.

Capabilities and Services

WLP



- Design services available
  - Layout
  - Mask tooling
- Wafer RDL patterning and bumping (ball sphere loaded or plated)
- Automated Optical Inspection (AOI) for best in class quality assurance
- Wafer map generation

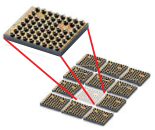
Inspect & Clean
PBO or PI 1
RDL Seed Deposition
Resist Processing
Cu RDL Plating
Resist & Seed Removal
PBO or PI 2
UBM Seed Deposition
Resist Processing
Cu or Ni-based UBM
Resist & Seed Removal
Ball Place

Test

Contact Probe

- Test software and hardware development
- Probe card design, service and support
- Test program transfer
- Wafer sort for RF, memory, logic and analog applications

DPS



Backgrind
Backside Lamination
Laser Mark
Singulation
Tape & Reel
AOI

- Best in class singulated device edge quality for all Si nodes
- Shipping material design and supply management
- Drop ship to final customer available

Visit Amkor Technology online for locations and to view the most current product information.

DS720H
Rev Date: 1/16